



**BUREAU
VERITAS**

Certificate of compliance

Applicant: SMA Solar Technology AG
Sonnenallee 1
34266 Niestetal
Germany

Product: Grid-tied battery storage inverter

Model: SBS2.5-1VL-10

Use in accordance with regulations:

Automatic disconnection device with single-phase mains surveillance in accordance with Engineering Recommendation G83/2 for photovoltaic systems with a single-phase parallel coupling via an inverter in the public mains supply. The automatic disconnection device is an integral part of the aforementioned inverter. This serves as a replacement for the disconnection device with isolating function that can access the distribution network provider at any time.

Applied rules and standards:

Engineering Recommendation G83/2:2012

Recommendations for the Connection of Type Tested Small-scale Embedded Generators (Up to 16A per Phase) in Parallel with Low-Voltage Distribution Systems

DIN V VDE V 0126-1-1:2006-02 (Functional safety)

Automatic disconnection device between a generator and the public low-voltage grid

At the time of issue of this certificate the safety concept of an aforementioned representative product corresponds to the valid safety specifications for the specified use in accordance with regulations.

Report number: 14TH0397-G83/2
Certificate number: U16-0259
Date of issue: 2016-05-20

Certification body



Deutsche
Akkreditierungsstelle
D-ZE-12024-01-00

Certification body of Bureau Veritas Consumer Products Services Germany GmbH
Accredited according to DIN EN ISO/IEC 17065

Appendix 4 Type Verification Test Report

Extract from test report according the Engineering Recommendation G83/2

Nr. 14TH0397

Type Approval and declaration of compliance with the requirements of Engineering Recommendation G83/2.

| | |
|----------------------------------|--|
| Manufacturer / applicant: | SMA Solar Technology AG Sonnenallee 1 34266 Niestetal Germany |
| SSEG Type | Grid-tied battery storage inverter |
| Rated values | SBS2.5-1VL-10 |
| Maximum rated capacity | 2500 VA |
| Rated voltage | 220/230/240 |
| Firmware version | 2.02 |
| Measurement period: | 2016-04-12 to 2016-05-19 |

Description of the electrical circuit

Special lockable battery connectors are provided to connect the DC source. An EMC filter consisting of x-, y-capacitors and an inductance is provided to remove distortions coming from the inverter to the DC side. The input current is measured via current sensors. The step up converters consist of inductances, transistors and diodes which increase the DC input voltage to the DC link which consists of electrolytic capacitors in parallel. The sine wave is generated from the IGBT bridges which receive a PWM signal from the internal processor. The generated sine is smoothed by inductances and routed through redundant relay contacts in each line to the output filter. For safety purposes a fault current and earth leakage monitoring is provided. The EMC filter consists of x-, y-capacitors and inductances

The above stated Small Scale Embedded Generators (SSEGs) are tested according the requirements in the Engineering Recommendation G83/2. Any modification that affects the stated tests must be named by the manufacturer/supplier of the product to ensure that the product meets all requirements of the Engineering Recommendation G83/2.

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| Protection. Voltage tests. | | | | | | |
|---|---------|------------|-----------|------------|------------------|-----------------|
| The requirement is specified in section 5.3.1, test procedure in Annex A or B 1.3.2 | | | | | | |
| Phase 1 | | | | | | |
| Function | Setting | | Trip test | | No trip test | |
| | Voltage | Time delay | Voltage | Time delay | Voltage / time | Confirm no trip |
| U/V stage 1 | 200,1V | 2,5s | 198,6V | 2,5261s | 204,1V / 3,5s | No trip |
| U/V stage 2 | 184V | 0,5s | 182,6V | 0,5275s | 188V / 2,48s | No trip |
| | | | | | 180V / 0,48s | No trip |
| O/V stage 1 | 262,2V | 1,0s | 261,2V | 1,0165s | 258,2V 2,0s | No trip |
| O/V stage 2 | 273,7V | 0,5s | 272,3V | 0,5275s | 269,7V 0,98s | No trip |
| | | | | | 277,7V 0,48s | No trip |

Note for Voltage tests the Voltage required to trip is the setting $\pm 3,45V$. The time delay can be measured at a larger deviation than the minimum required to operate the protection. The No trip tests need to be carried out at the setting $\pm 4V$ and for the relevant times as shown in the table above to ensure that the protection will not trip in error.

| Protection. Frequency tests. | | | | | | |
|---|-----------|------------|-----------|------------|--------------------|-----------------|
| The requirement is specified in section 5.3.1, test procedure in Annex A or B 1.3.3 | | | | | | |
| Function | Setting | | Trip test | | No trip test | |
| | Frequency | Time delay | Frequency | Time delay | Frequency / time | Confirm no trip |
| U/F stage 1 | 47,5Hz | 20s | 47,50Hz | 20,05s | 47,7Hz / 25s | No trip |
| U/F stage 2 | 47Hz | 0,5s | 47,00Hz | 0,532s | 47,2Hz / 19,98s | No trip |
| | | | | | 46,8Hz / 0,48s | No trip |
| O/F stage 1 | 51,5Hz | 90s | 51,51Hz | 90,02s | 51,3Hz / 95s | No trip |
| O/F stage 2 | 52Hz | 0,5s | 52,01Hz | 0,5325s | 51,8Hz / 89,98s | No trip |
| | | | | | 52,2Hz / 0,48s | No trip |

Note for Frequency Trip tests the Frequency required to trip is the setting $\pm 0,1Hz$. In order to measure the time delay a larger deviation than the minimum required to operate the projection can be used. The "No-trip tests" need to be carried out at the setting $\pm 0,2Hz$ and for the relevant times as shown in the table above to ensure that the protection will not trip in error.

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Protection. Loss of Mains.

The requirement is specified in section 5.3.2, test procedure in Annex A or B 1.3.4

Note as an alternative, inverters can be tested to BS EN 62116. The following sub set of tests should be recorded in the following table.

| | | | | | | |
|---|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|-----------------------------|
| Balancing load on islanded network | 33% of -5% Q Test 22 | 66% of -5% Q Test 12 | 100% of -5% P Test 5 | 33% of +5% Q Test 31 | 66% of +5% Q Test 21 | 100% of +5% P Test 10 |
| Trip time. Ph1 fuse removed | 170ms | 176ms | 210ms | 188ms | 188ms | 191ms |

Note for technologies which have a substantial shut down time this can be added to the 0,5 seconds in establishing that the trip occurred in less than 0,5s. Maximum shut down time could therefore be up to 1,0 seconds for these technologies.

Indicate additional shut down time included in above results.
(Integrated interface switch)

Type of switching equipment 1:
ZETTLER electronics AZ733W-2A-12DE with 10ms
Type of switching equipment 2:
ZETTLER electronics AZ733W-2A-12DE with 10ms

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| Protection. Re-connection timer. | | | | | |
|---|-----------------|---|-----------------|-----------------|-----------|
| The requirement is specified in section 5.3.4 Automatic Reconnection, test procedure in Annex A or B 1.3.5 | | | | | |
| Test should prove that the reconnection sequence starts after a minimum delay of 20 seconds for restoration of voltage and frequency to within the stage 1 settings of table 1. | | | | | |
| Voltage | | | | | |
| Time delay setting | | Measured delay | | | |
| 20s | | 23,44 | | | |
| Frequency | | | | | |
| Time delay setting | | Measured delay | | | |
| 20s | | 23,44 | | | |
| | | Checks on no reconnection when voltage or frequency is brought to just outside stage 1 limits of table 1. | | | |
| | | At 266,2V | At 196,1V | At 47,4Hz | At 51,6Hz |
| Confirmation that the SSEG does not re-connect. | No reconnection | No reconnection | No reconnection | No reconnection | |

| Protection. Frequency change, Stability test. | | | | |
|--|----------------------------|---------------|--------------------------|------------------------|
| The requirement is specified in section 5.3.3, test procedure in Annex A or B 1.3.6 | | | | |
| | Start Frequency | Change | End Frequency | Confirm no trip |
| Positive Vector Shift | 49,5Hz | +9 degrees | | No Trip |
| Negative Vector Shift | 50,5Hz | - 9 degrees | | No Trip |
| Positive Frequency drift | 49,5Hz | +0,19Hz/sec | 51,5Hz | No Trip |
| Negative Frequency drift | 50,5Hz | -0,19Hz/sec | 47,5Hz | No Trip |

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| Power Quality. Harmonics. | | | | | | |
|---|------------------------------------|-------------------------------|-------------------------------|-------------------------------|---------------------------------|---|
| The requirement is specified in section 5.4.1, test procedure in Annex A or B 1.4.1 | | | | | | |
| Phase 1 | | | | | | |
| SSEG rating per phase (rpp) | | | | NV=MV*3,68/rpp | | |
| | At 45-55% of rated ouput 1,25kW | | 100% of rated output 2,5kW | | | |
| Harmonic | Measured Value (MV) in Amps | Normalised Value (NV) in Amps | Measured Value (MV) in Amps | Normalised Value (NV) in Amps | Limit in BS EN61000-3-2 in Amps | Higher limit for odd harmonics 21 and above |
| 2nd | 0,020 | 0,089 | 0,025 | 0,111 | 1,080 | |
| 3rd | 0,048 | 0,213 | 0,96 | 0,426 | 2,300 | |
| 4th | 0,003 | 0,013 | 0,002 | 0,009 | 0,430 | |
| 5th | 0,029 | 0,129 | 0,035 | 0,155 | 1,140 | |
| 6th | 0,003 | 0,013 | 0,002 | 0,009 | 0,300 | |
| 7th | 0,019 | 0,084 | 0,023 | 0,102 | 0,770 | |
| 8th | 0,002 | 0,009 | 0,002 | 0,009 | 0,230 | |
| 9th | 0,014 | 0,062 | 0,015 | 0,067 | 0,400 | |
| 10th | 0,002 | 0,009 | 0,002 | 0,009 | 0,184 | |
| 11th | 0,012 | 0,053 | 0,009 | 0,040 | 0,330 | |
| 12th | 0,001 | 0,004 | 0,002 | 0,009 | 0,153 | |
| 13th | 0,012 | 0,053 | 0,011 | 0,049 | 0,210 | |
| 14th | 0,131 | 0,001 | 0,004 | 0,001 | 0,131 | |
| 15th | 0,150 | 0,011 | 0,049 | 0,010 | 0,150 | |
| 16th | 0,115 | 0,001 | 0,004 | 0,001 | 0,115 | |
| 17th | 0,132 | 0,010 | 0,044 | 0,010 | 0,132 | |
| 18th | 0,102 | 0,001 | 0,004 | 0,001 | 0,102 | |
| 19th | 0,118 | 0,008 | 0,035 | 0,007 | 0,118 | |
| 20th | 0,092 | 0,001 | 0,004 | 0,001 | 0,092 | |
| 21th | 0,107 | 0,007 | 0,031 | 0,007 | 0,107 | 0,160 |
| 22th | 0,084 | 0,001 | 0,004 | 0,001 | 0,084 | |
| 23th | 0,098 | 0,006 | 0,027 | 0,007 | 0,098 | 0,147 |
| 24th | 0,077 | 0,001 | 0,004 | 0,001 | 0,077 | |
| 25th | 0,090 | 0,005 | 0,022 | 0,008 | 0,090 | 0,135 |
| 26th | 0,071 | 0,001 | 0,004 | 0,001 | 0,071 | |
| 27th | 0,083 | 0,003 | 0,013 | 0,008 | 0,083 | 0,124 |
| 28th | 0,066 | 0,001 | 0,004 | 0,001 | 0,066 | |
| 29th | 0,078 | 0,003 | 0,013 | 0,007 | 0,078 | 0,117 |
| 30th | 0,061 | 0,001 | 0,004 | 0,001 | 0,061 | |
| 31th | 0,073 | 0,002 | 0,009 | 0,006 | 0,073 | 0,109 |
| 32th | 0,058 | 0,001 | 0,004 | 0,001 | 0,058 | |
| 33th | 0,058 | 0,001 | 0,009 | 0,006 | 0,068 | 0,102 |
| 34th | 0,054 | 0,001 | 0,004 | 0,001 | 0,054 | |
| 35th | 0,064 | 0,001 | 0,004 | 0,007 | 0,064 | 0,096 |
| 36th | 0,051 | 0,001 | 0,004 | 0,001 | 0,051 | |
| 37th | 0,061 | 0,002 | 0,009 | 0,007 | 0,061 | 0,091 |
| 38th | 0,048 | 0,001 | 0,004 | 0,001 | 0,048 | |
| 39th | 0,058 | 0,004 | 0,013 | 0,007 | 0,058 | 0,087 |
| 40th | 0,046 | 0,001 | 0,004 | 0,001 | 0,046 | |

Note the higher limits for odd harmonics 21 and above are only allowable under certain conditions, if these higher limits are utilised please state the exemption used as detailed in part 6.2.3.4 of BS EN 61000-3-2 in the box below.

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Power Quality. Power factor.

The requirement is specified in section 5.6, test procedure in Annex A or B 1.4.2

| | | | | |
|----------------|--------|-------|-------|---|
| | 216,2V | 230V | 253V | Measured at three voltage levels and at full output. Voltage to be maintained within $\pm 1.5\%$ of the stated level during the test. |
| Measured value | 0,999 | 0,999 | 0,999 | |
| Limit | >0,95 | >0,95 | >0,95 | |

Power Quality. Voltage fluctuation and Flicker.

The requirement is specified in section 5.4.2, test procedure in Annex A or B 1.4.3

| | Starting | | | Stopping | | | Running | |
|--|----------|------|---------------|----------|------|---------------|---------|-------------|
| | dmax | dc | d(t) | dmax | dc | d(t) | Pst | Plt 2 hours |
| Measured values | 0,2% | 0,1% | 0 | 0,0% | 0,0% | 0 | 0,07 | 0,07 |
| Normalised to standard impedance and 3.68kW for multiple units | 0,7% | 0,1% | 0 | 0,0% | 0,0% | 0 | 0,31 | 0,31 |
| Limits set under BS EN 61000-3-3 | 4% | 3,3% | 3,3% 500ms | 4% | 3,3% | 3,3% 500ms | 1,0 | 0,65 |

Power Quality. DC injection.

The requirement is specified in section 5.5, test procedure in Annex A or B 1.4.4

| | | | |
|----------------------------------|--------|--------|--------|
| Test level power | 10% | 55% | 100% |
| Recorded value of phase 1 | 3 mA | 2 mA | 8 mA |
| As % of rated AC current phase 1 | 0,03 % | 0,01 % | 0,08 % |
| Limit | 0,25% | 0,25% | 0,25% |

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Fault level Contribution.

The requirement is specified in section 5.7, test procedure in Annex A or B 1.4.6

| For a directly coupled SSEG | | | For a Inverter SSEG | | |
|--|----------|-------|---------------------|-------|------------|
| Parameter | Symbol | Value | Time after fault | Volts | Amps |
| Peak Short Circuit current | I_p | N/A | 20ms | 230,3 | 12,76 |
| Initial Value of aperiodic current | A | N/A | 100ms | 12,59 | 0,04 |
| Initial symmetrical short-circuit current* | I_k | N/A | 250ms | 10,35 | 0,04 |
| Decaying (aperiodic) component of short circuit current* | i_{DC} | N/A | 500ms | 11,35 | 0,04 |
| Reactance/Resistance Ratio of source* | X/R | N/A | Time to trip | 0,52 | In seconds |

For rotating machines and linear piston machines the test should produce a 0s – 2s plot of the short circuit current as seen at the Generating Unit terminals.

* Values for these parameters should be provided where the short circuit duration is sufficiently long to enable interpolation of the plot.

Self Monitoring – Solid state switching.

The requirement is specified in section 5.3.1, No specified test requirements.

N/A

It has been verified that in the event of the solid state switching device failing to disconnect the SSEG, the voltage on the output side of the switching device is reduced to a value below 50 volts within 0,5 seconds.

Note. Unit do not provide solid state switching relays. In case the semiconductor bridge is switched off, then the voltage on the output drops to 0. In this case the relays on the output will also open.